ABSTRACT OF THE DISCLOSURE

A data processing machine including a CPU which is configured to operate with an adjustable (variable) clock frequency. The clock frequency is adjusted in accordance with a clock change request signal. A plurality of clock change request signals have respective priority orders. A plurality of clock frequencies are prepared for the clock change request signals. When two or more clock change request signals are input, one of them is selected based on the priority order. The clock signal (clock frequency) to be applied to the CPU is changed in accordance with the selected clock change request signal. The data processing machine can adjust a timing for memory access to an optimal timing when the clock frequency is adjusted. The data processing machine can also deal with various clock frequency change requests.